

Design and Simulation of First Order Sigma-Delta Modulator Using LT spice Tool

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ABSTRACT

A switched-capacitor single-stage Sigma-Delta ADC with a first-order modulator is proposed. Efficient low power first Order 1-Bit Sigma-Delta ADC designed which accepts input signal bandwidth of 10 MHz. This circuitry performs the function of an analog-to-digital converter. A first-order 1-Bit Sigma-Delta (Σ - Δ) modulator is designed, simulated and analyzed using LTspice standard 250nm CMOS technology power supply of 1.8V. The modulator is proved to be robustness, the high performance in stability. The simulations are compared with those from a traditional analog-to-digital converter to prove that Sigma-Delta is performing better with low power and area.

Keywords - 1-Bit Sigma-Delta ADC, CMOS Technology, LTspice Tool.

I. INTRODUCTION

Transistor scaling has been the driving force for technology advancements in the semiconductor industry over the last few decades. The main driver for the semiconductor industry has been Moore's law where the doubling of transistors has led to phenomenal increase in functionality of the integrated circuit (IC). Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. This incredible growth has come from steady miniaturization of transistors and improvements in manufacturing processes. A/D (Analog-to-Digital) converter is a device, which translates an analog voltage signal into a corresponding digital number. Whenever we relate to the real world most of the signals are analog in nature. But some applications such as digital signal processing requires signals to be digital. The technological improvement in digital VLSI circuits has increased the need for low cost high performance A/D and D/A (Digital-to-Analog) converters, where a considerable amount of analog circuitry is integrated with digital circuitry. Unfortunately, marrying sensitive analog circuitry and digital circuitry on a single chip has been a difficult task due to the noise coupling problems. Sigma-Delta modulation (SDM) was developed to overcome the limitations of delta modulation. Sigma-Delta systems quantize the delta (difference) between the current signal and the sigma (sum) of the previous difference.

II. OPTIMUM TOPOLOGY OF SIGMA-DELTA ARCHITECTURE

Oversampling converters typically employ switched-capacitor circuits and therefore do not need sample and hold circuits. Sigma-Delta modulators shown in the figure 1; come under the over sampling converters. The comparator compares the input signal against its last sample, to see if this new sample is larger than the last one. If it is larger, then the output is increasing and if it is smaller, then the output is decreasing. As the Greek letter- Δ (delta) is used to show the deviation or small incremental change, the process came to be known as "delta modulation". Delta modulation is based on quantizing the change in the signal from sample to sample rather than the absolute value of the signal at each sample. Sigma stands for summing or integrating, which is performed at the input stage on the digital output with the input signal before the delta modulation as shown in figure 1; hence the analog to digital conversion of this technique is called "Sigma-Delta modulation". 1st order Sigma-Delta modulator design of figure 1; consists of mainly an integrator. The number of integrators in the forward path determines the order of the modulator. The output of the comparator is fed back through a 1-Bit DAC to the summing input. The negative feedback loop from the comparator output through the 1-Bit DAC back to the summing point will force the average voltage to be equal to V_{IN} . This implies that the average DAC output voltage must equal the input voltage V_{in} . The 1-Bit DAC is a simple multiplexer circuit controlled by the output of the comparator to determine if $+V_{ref}$ or $-V_{ref}$ is summed with the input. When the integrator output is greater than the reference voltage at the comparator input, the comparator gives an output 'high'. This output high controls the DAC which gives an output

of +Vref which is subtracted from the input of the modulator in order to move the integrator output in the negative direction. Similarly when the Integrator output is less than the reference voltage at the comparator input, the feedback path moves the integrator output in the positive direction. The integrator therefore accumulates the difference between the input and quantized output signals and tries to maintain the integrator output around zero.

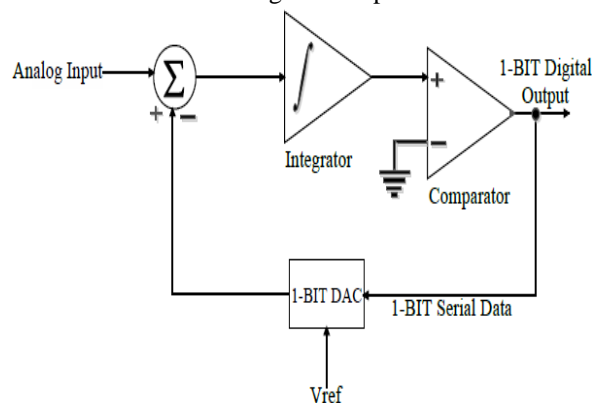


Fig 1: 1-Bit Sigma-Delta Modulator

III. DESIGN OF OPERATIONAL AMPLIFIER

Operational Amplifier (Op-amp) is the core part of the Sigma-Delta modulator. It provides a large open loop gain to implement the negative feedback concept as well as let the integrator integrate smoothly. In addition, it has large bandwidth to pass through at least the first two harmonics of input sine wave. The op-amp operates at the clock frequency, since the differences are being integrated over the region of time. Therefore, to effectively pass the signal at the clock frequency the gain bandwidth product of the op-amp must be greater than one. The amplifier used is shown in figure 2. The first stage consists of p-channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M7. The first stage gives a high differential gain and performs the differential to single ended conversion. This stage gives a good differential gain and also performs the differential to single-ended conversion. The second stage consists of an n-channel common-source amplifier M5 with a p-channel current load M6. The bias of the Op-Amp circuit is provided by M8 and M9 transistors. By using the combination of transistor M8 and M9 which is equivalent to a standard resistor diode (gate tied to drain) combination, a reference current is obtained, which is designed to produce a current of 100 μ A. The voltage swing of op-amp is +2V to -2V, Gain Bandwidth (GB) is 10MHz; output resistance is 1K Ω , and power dissipation is 18.23 μ w. The Frequency response of Op-Amp is shown in figure 3.

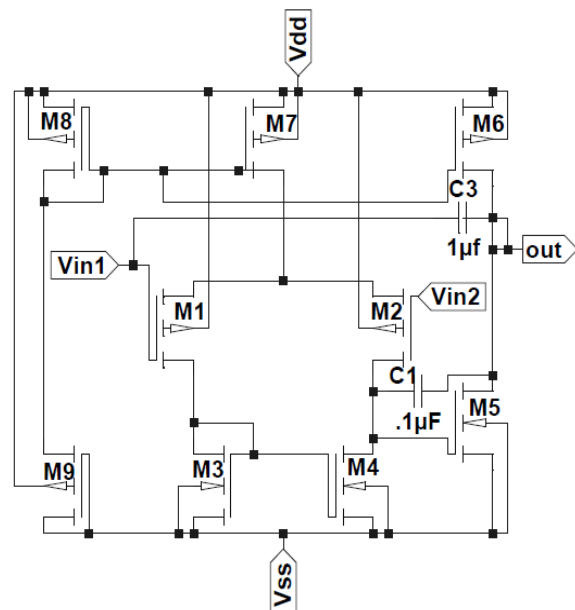


Fig 2: Schematic view of Operational Amplifier

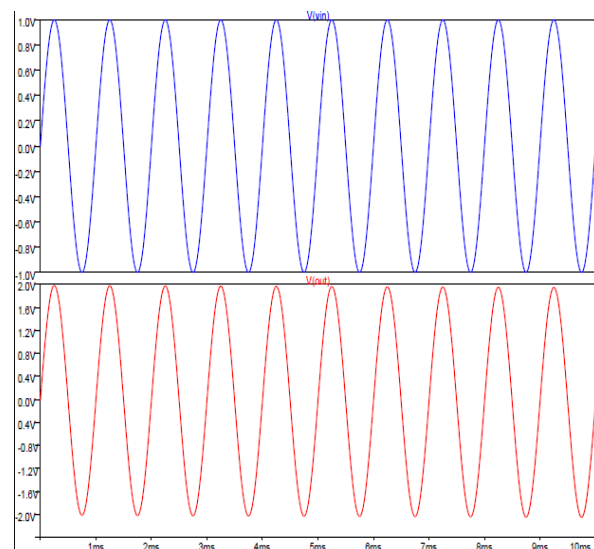


Fig 3: The frequency response of Op-Amp (Input & Output)

IV. DESIGN OF COMPARATOR

A comparator acts as the quantizer in the first order modulator. Since the comparator is of 1-bit it has only two levels either a '1' or a '0'. A '1' implies that $V_{in} > V_{ref}$ and a '0' implies that $V_{in} < V_{ref}$. If the output of the integrator is greater than the reference voltage (V_{ref}) it has to give an output of '1', and if the integrator output is less than reference voltage then the output of the comparator should be '0'. A simple comparator performs the required function efficiently. The operational amplifier can be used as a comparator. The only change needed is that the comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow

down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail. The slew rate for the comparator is measured by giving a step input signal and measuring the time it takes for the comparator to reach the final output value. The clock frequency of the first order modulator depends on the slew rate of the comparator. The clock frequency should be less than the slew rate of the comparator. The clock takes half cycle to switch from -2.5V to +2.5V. The maximum allowed clock frequency for the above slew rate would be 10 MHz. When the clock frequency is more than 10 MHz, the comparator output will be distorted. Fig. 5 shows the transient response of the comparator with 0.5v dc offset.

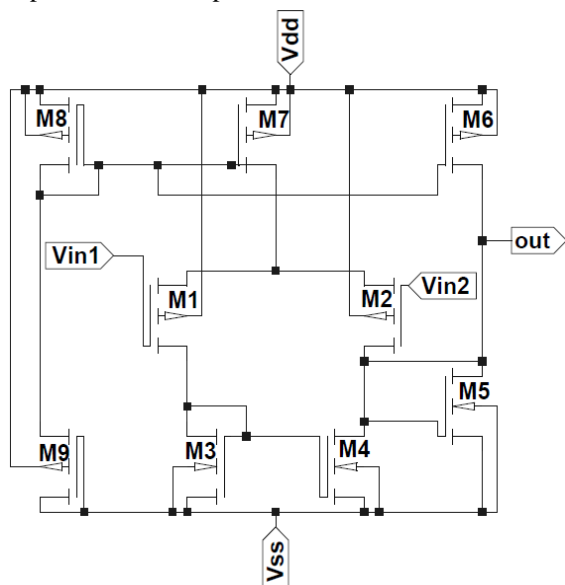


Fig 4: Schematic view of Comparator

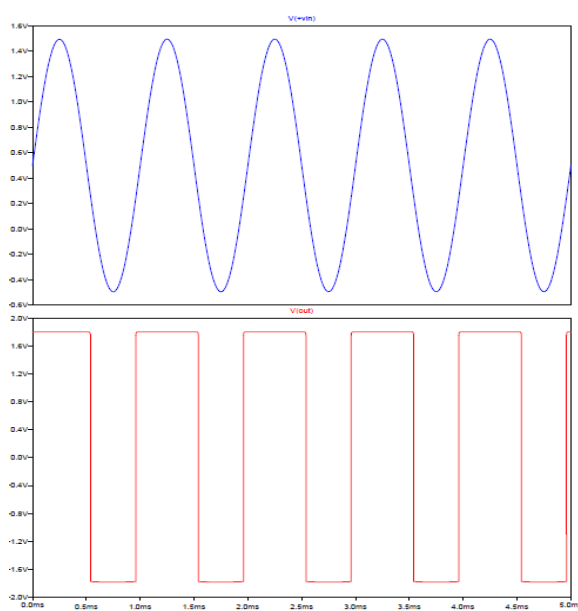


Fig 5: The frequency response of Comparator (Input & Output)

V. DESIGN OF 1-BIT DAC

The designed comparator, as a two-stage CMOS operational amplifier, will give an output of 1-bit digital input to the digital to analog converter. A 1-Bit digital-to-analog converter converts the 1-bit digital output of the comparator to the analog signal and this analog signal, fed back to the SC-integrator again. The DAC consists of two transmission gates. The input to each transmission gate is a voltage divided down from the positive and negative 2.5 volt rails which acts as $\pm V_{ref}$ signals depending on the 1-Bit digital input signal. The most important component of feedback path is the 1 bit DAC that converts the output digital bit stream to analog value based on a reference voltage. The DAC used is shown in figure 6. The present 1-Bit digital-to-analog converter has two reference voltages a positive reference voltage of $+V_{ref} = +2.5v$ and a negative reference voltage of $-V_{ref} = -2.5v$ the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted. Frequency response of digital to analog converter is shown in figure 7. A 1-bit digital to analog converter can be designed using a simple multiplexer circuit, which selects between the $+V_{ref}$ and $-V_{ref}$ signals depending on the 1-bit digital input signal.

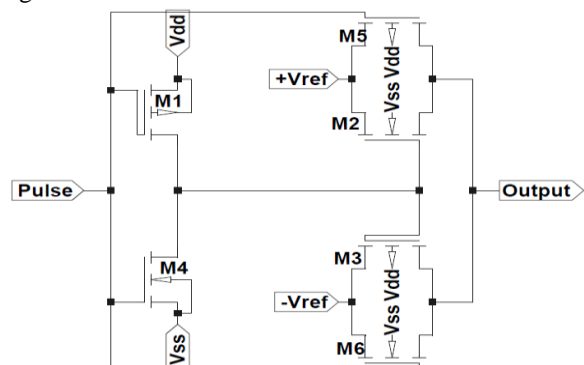


Fig 6: Schematic view of DAC

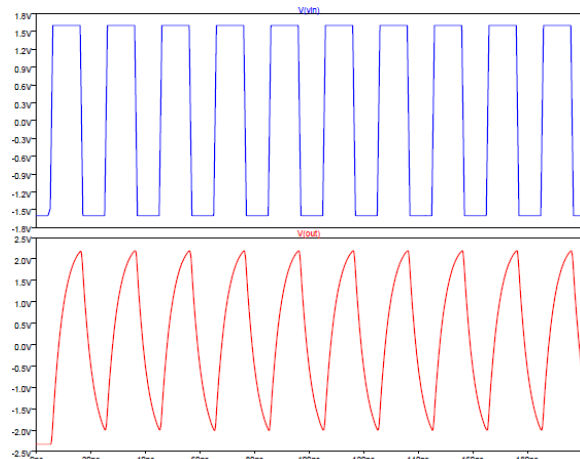


Fig 7: The frequency response of DAC (Input & Output)

VI. SIMULATION RESULT

The theoretical results are obtained from post-layout LTspice (Linear Technology LTspice IV 4.21b, SPICE Simulator) simulations using SPICE level-1 MOS model parameters. The circuit design of Op-amp, Comparator and DAC for first order Sigma-Delta (Σ - Δ ADC) have been developed and implemented by using 250nm CMOS Technology. The frequency response of Sigma-Delta ADC is shown in figure 8. The whole First order Sigma-Delta ADC subsystem works very well under the following conditions:

Input sine wave frequency up to 10MHz.
Supply Voltage to Vdd=+1.8V and Vss= -1.8V
Power Dissipation is 35.426 μ w
System noise is 6.15n \sqrt{H}

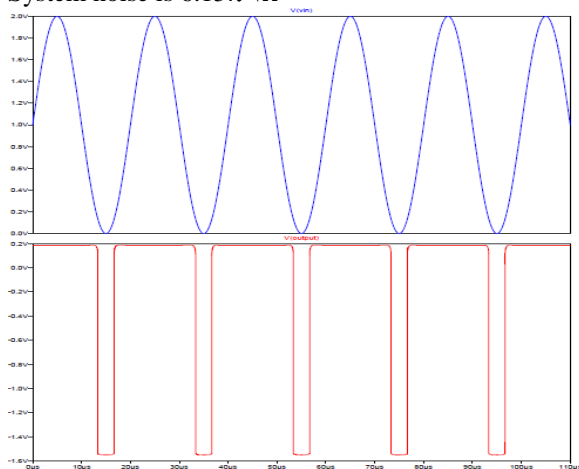


Fig 8: The frequency response of 1-BitSigma-Delta ADC

VII. CONCLUSION

A 1-Bit first order Sigma-Delta ADC has been designed in standard 250nm n-well CMOS technology. The results demonstrate that the usage of a Sigma-Delta modulator allows very weak analog signals to be converted to an extremely high resolution digital output. It has been shown that switched-capacitor circuits are a viable approach to the design of low voltage, high-resolution Sigma-Delta modulators, even when only high threshold voltage transistors are available. It has been noted that the reduction of the oversampling ratio has limited benefit for the reduction of the modulator power dissipation.

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